

1.5V Drive Pch+Pch MOSFET

QS8J1

●Structure

Silicon P-channel MOSFET

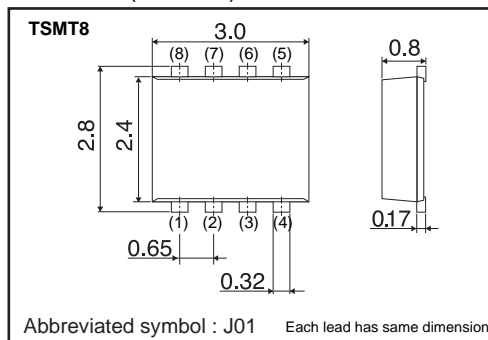
●Features

- 1) Low On-resistance.
- 2) Low voltage drive. (1.5 V)
- 3) High power package.

●Applications

Switching

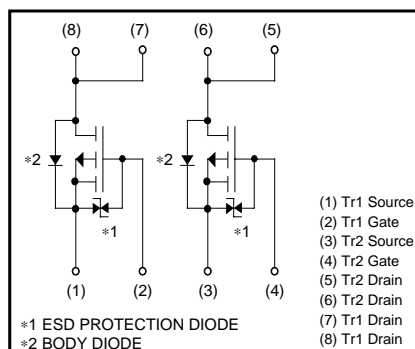
●Dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TR
QS8J1		○
	Basic ordering unit (pieces)	3000

●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	-12	V	
Gate-source voltage	V_{GSS}	±10	V	
Drain current	Continuous	I_D	±4.5	A
	Pulsed	I_{DP} *1	±18	A
Source current (Body diode)	Continuous	I_S	-1	A
	Pulsed	I_{SP} *1	-18	A
Total power dissipation	P_D *2	1.5	W / TOTAL	
		1.25	W / ELEMENT	
Channel temperature	T_{ch}	150	°C	
Range of Storage temperature	T_{stg}	-55 to +150	°C	

*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	83.3	°C/W / TOTAL
		100	°C/W / ELEMENT

* Mounted on a ceramic board.

Transistors

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} =±10V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	–12	–	–	V	I _D = –1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	–1	μA	V _{DS} = –12V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	–0.3	–	–1.0	V	V _{DS} = –6V, I _D = –1mA
Static drain-source on-state resistance	R _{DS(on)} *	–	21	29	mΩ	I _D = –4.5A, V _{GS} = –4.5V
		–	27	38	mΩ	I _D = –2.2A, V _{GS} = –2.5V
		–	36	54	mΩ	I _D = –2.2A, V _{GS} = –1.8V
		–	49	98	mΩ	I _D = –0.9A, V _{GS} = –1.5V
Forward transfer admittance	Y _{fs} *	6.5	–	–	S	V _{DS} = –6V, I _D = –4.5A
Input capacitance	C _{iss}	–	2450	–	pF	V _{DS} = –6V
Output capacitance	C _{oss}	–	320	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	290	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	–	12	–	ns	V _{DD} ≐ –6V
Rise time	t _r *	–	75	–	ns	V _{GS} = –4.5V I _D = –2.2A
Turn-off delay time	t _{d(off)} *	–	390	–	ns	R _L ≐ 2.7Ω
Fall time	t _f *	–	215	–	ns	R _G =10Ω
Total gate charge	Q _g *	–	31	–	nC	V _{DD} ≐ –6V V _{GS} = –4.5V
Gate-source charge	Q _{gs} *	–	4.5	–	nC	I _D = –4.5A
Gate-drain charge	Q _{gd} *	–	4.0	–	nC	R _L ≐ 1.3Ω / R _G =10Ω

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	–	–	–1.2	V	I _S = –4.5A, V _{GS} =0V

* Pulsed

Transistors

●Electrical characteristic curves

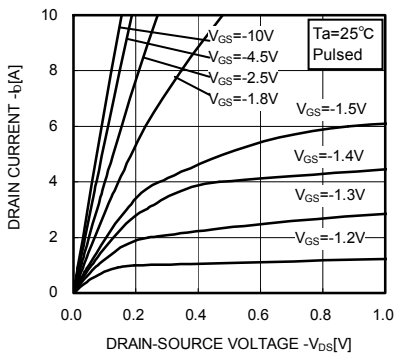


Fig.1 Typical Output Characteristics (I)

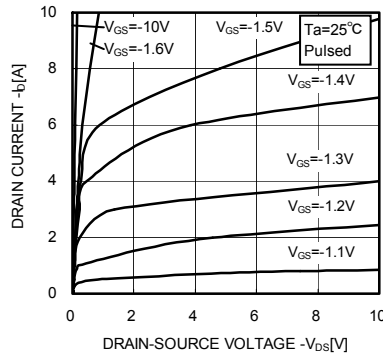


Fig.2 Typical Output Characteristics (II)

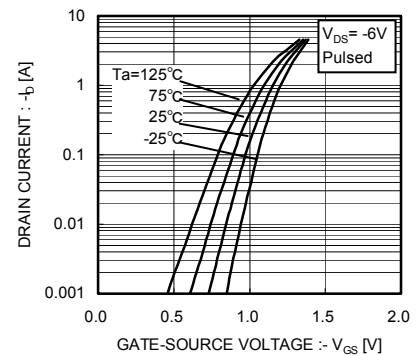


Fig.3 Typical Transfer Characteristics

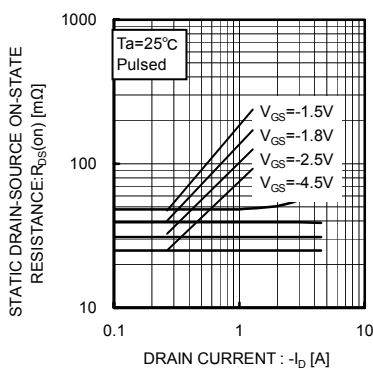


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

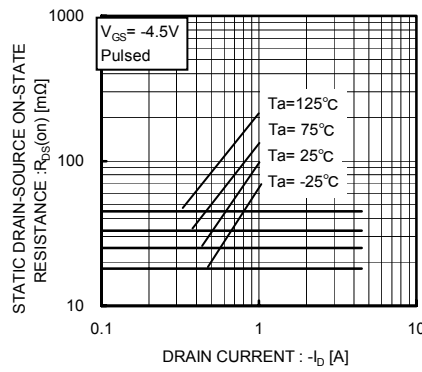


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

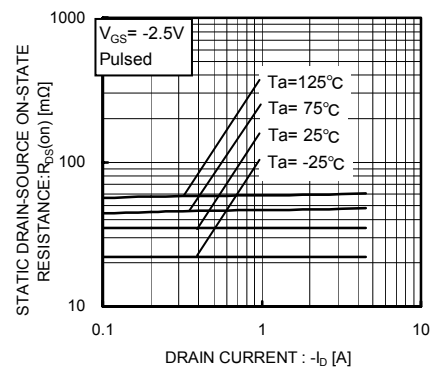


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

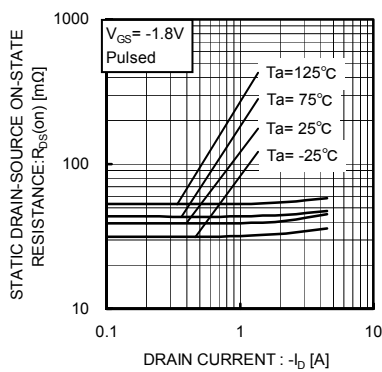


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

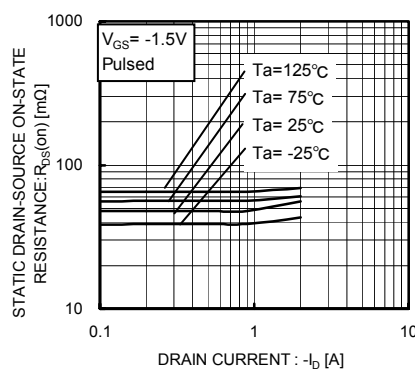


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (V)

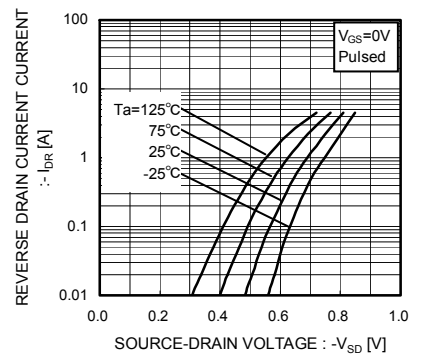


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

Transistors

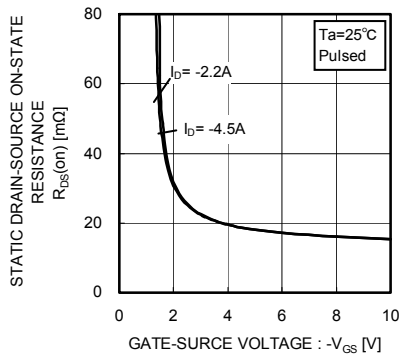


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

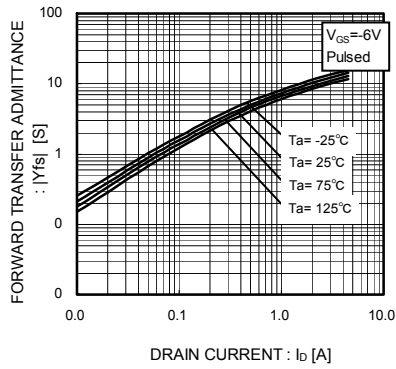


Fig.11 Forward Transfer Admittance vs. Drain Current

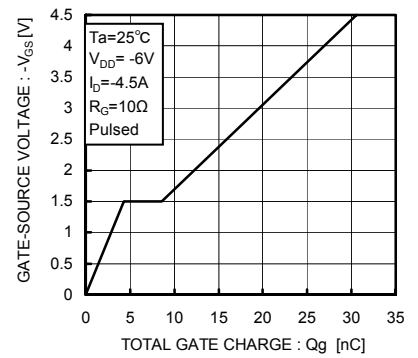


Fig.12 Dynamic Input Characteristics

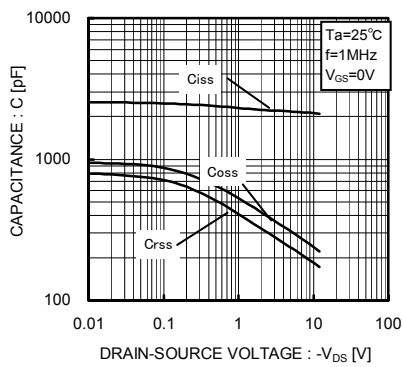


Fig.13 Typical Capacitance vs. Drain-Source Voltage

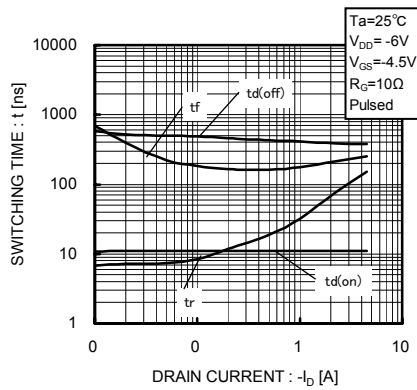


Fig.14 Switching Characteristics

Transistors

●Measurement circuits

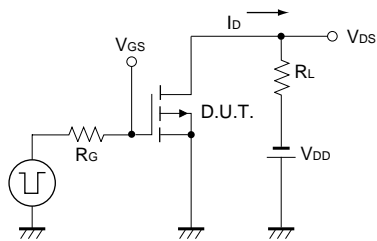


Fig.1-1 Switching Time Measurement Circuit

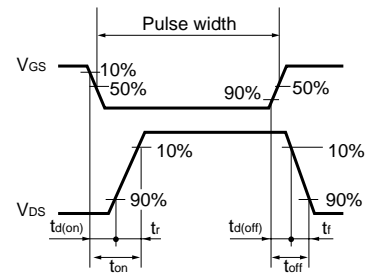


Fig.1-2 Switching Time Waveforms

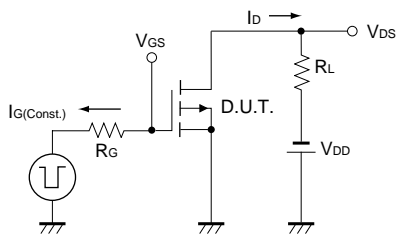


Fig.2-1 Gate Charge Measurement Circuit

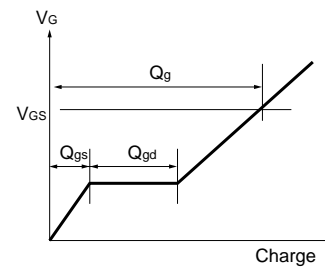


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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