STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT NAME	White LED driver for car navigation back light
TYPE	**BD8118FM**

FEATURES

- Step-up DC/DC converter
- Built in OSC
- Built in UVLO
- Built in OVP
- 4 parallel current output（output current is set with external resister）
- LED open detection circuit
- Built in TSD
- PWM adjustment
- Built in OCP
- FAIL output（self diagnosis）

●ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	LIMITS	UNIT
Power supply voltage(Pin : 1)	V_{CC}	36	V
Load switch output voltage(Pin : 2)	V_{LOADSW}	36	V
LED output voltage(Pin : 12, 14, 15, 17)	V_{LED}	36	V
FAIL output voltage(Pin : 3, 20)	V_{OL}	7	V
Input voltage(Pin : 5, 6, 10, 11, 24)	V_{IN}	−0.3〜7 < VCC	V
VDAC input voltage(Pin : 8)	V_{DAC}	−0.3〜7 < VCC	V
Power dissipation	Pd	2.20 ※1	W
Junction Temperature	Tjmax	150	℃
Operating temperature range	Topr	−40〜+95	℃
Strage temperature range	Tstg	−55〜+150	℃
LED drive current(Pin : 12, 14, 15, 17)	I_{LED}	150 ※2※3	mA

※1　70mm×70mm×1.6mm glass epoxy mounting. Decline by 17.6mw/℃
※2　It is correlate LED drive current with　VF dispersion each of current outputs. Refer to the technical note.
※3　Current maximum for 1ch. Do not however exceed Pd.

●Operating range(Ta=25℃)

PARAMETER	SYMBOL	LIMITS	UNIT
Power Supply Voltage（Pin : 1)	V_{CC}	4.5〜30	V
Oscillation frequency(Pin : 26)	F_{OSC}	50〜550	kHz
External synchronous frequency(Pin : 6) ※4 ※5	F_{SYNC}	fosc〜550	kHz
External synchronous pulse(Pin : 6)	F_{SDUTY}	40〜60	%

※4　SYNC have to be connected to GND when external synchronizing frequency is not needed.
※5　Don't change external synchronous frequency to internal oscillation frequency when external synchronous frequency is inputted.

＊This product is not designed for protection against radioactive rays.

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● ELECTRICAL CHARACTERISTICS（Unless otherwise specified Ta=25℃, VCC=12V）

| PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		Min	Typ	Max		
Circuit current	I_{CC}	2.5	6	10	mA	EN=2V, SYNC=VREG, RT=OPEN PWM=OPEN, ISET=OPEN, C_{IN}=1μF
Standby current	I_{ST}	−	0	2	μA	EN=Low
[VREG] (Pin : 4)						
VREG output voltage	V_{REG}	4.5	5	5.5	V	I_{REG}=−10mA, C_{REG}=1μF
[SW] (Pin : 22, 23)						
SWOUT upper ON resistance	R_{ONH}	0.05	3	7	Ω	I_{ON}=−10mA
SWOUT lower ON resistance	R_{ONL}	0.05	2	5	Ω	I_{ON}=10mA
Over current protection limited voltage	V_{DCS}	0.3	0.4	0.5	V	V_{CS}=sweep up
[error amp] (Pin : 12, 14, 15, 17, 27, 28)						
LED control voltage	V_{LED}	0.7	0.8	0.9	V	
COMP shink current	I_{SKCP}	40	100	200	μA	V_{LED}=2V, Vcomp=1V
COMP source current	I_{SCCP}	−200	−100	−40	μA	V_{LED}=0V, Vcomp=1V
SS charge current	I_{SS}	−14	−10	−6	μA	V_{SS}=1.0V
SS maximum voltage	V_{MXSS}	2	2.5	3	V	EN=High
SS standby current	I_{STSS}	−	0	2	μA	EN=Low
[frequency] (Pin : 23, 26)						
Oscillation frequency	F_{OSC}	250	300	350	KHz	R_T=100kΩ
[OVP] (Pin : 25)						
Over voltage detection voltage	V_{DOVP}	1.86	2.0	2.14	V	VOVP=Sweep up
OVP hysteresis range	V_{DOHS}	0.35	0.45	0.55	V	VOVP=Sweep down
[UVLO] (Pin : 4)						
UVLO detection voltage	V_{DUVLO}	2.5	2.8	3.1	V	VREG=Sweep down
UVLO Hysteresis range	V_{DUHS}	50	100	200	mV	VREG=Sweep up
[Load SW] (Pin : 2)						
Load sw low voltage	V_{LDL}	0.05	0.15	0.3	V	I_{LOAD}=10mA
[LED output] (Pin : 5, 9, 12, 14, 15, 17, 25)						
LED current relative dispersion width	ΔI_{LED1}	−6	0	6	%	I_{LED}=50mA
LED current absolute dispersion width	ΔI_{LED2}	0	3	6	%	I_{LED}=50mA
ISET voltage	V_{ISET}	1.96	2.00	2.04	V	I_{LED}=50mA
PWM frequency	Duty	0.38	−	99.5	%	F_{PWM}=150Hz, I_{LED}=50mA ※1, 2, 3
PWM adjustment	F_{PWM}	0	−	20	KHz	Duty=50%, I_{LED}=50mA ※2, 3
Open detection voltage1	V_{DOP1}	0.05	0.15	0.3	V	VLED= Sweep down, VOVP＞VDOP2, VSS≧VMXSS
Open detection voltage2	V_{DOP2}	1.56	1.7	1.84	V	VOVP= Sweep up, VLED＞VDOP1, VSS≧VMXSS
[Logic input] (Pin : 5, 6, 10, 11, 24)						
Input high voltage	V_{INH}	2.6	−	5.5	V	
Input low voltage	V_{INL}	GND	−	0.8	V	
Input current	I_{IN}	18	35	53	μA	V_{IN}=5V (Pin : 5, 6, 10, 11)
Input current	I_{EN}	13	25	38	μA	V_{EN}=5V (Pin : 24)
[FAIL output] (Pin : 3, 20)						
FAIL low voltage	V_{FLL}	0.05	0.1	0.2	V	I_{OL}=1mA

◎ This product is not designed for protection against radioactive rays.

※1 0%, 100% input possible
※2 ILED=VDAC÷RISET×3300
※3 ILED=VISET÷RISET×3300, VDAC＞VISET

● PHYSICAL DIMENSIONS・MARKING

Product series

BD8118FM

Lot No.

HSOP−M28 （UNIT:mm）

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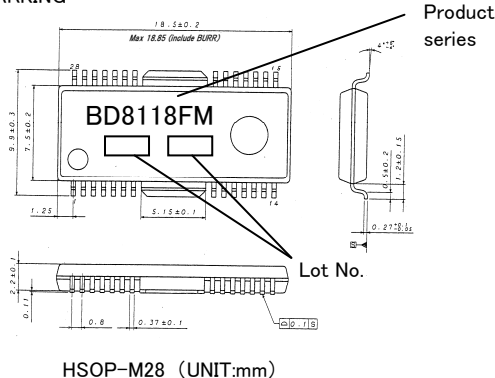
●BLOCK DIAGRAM
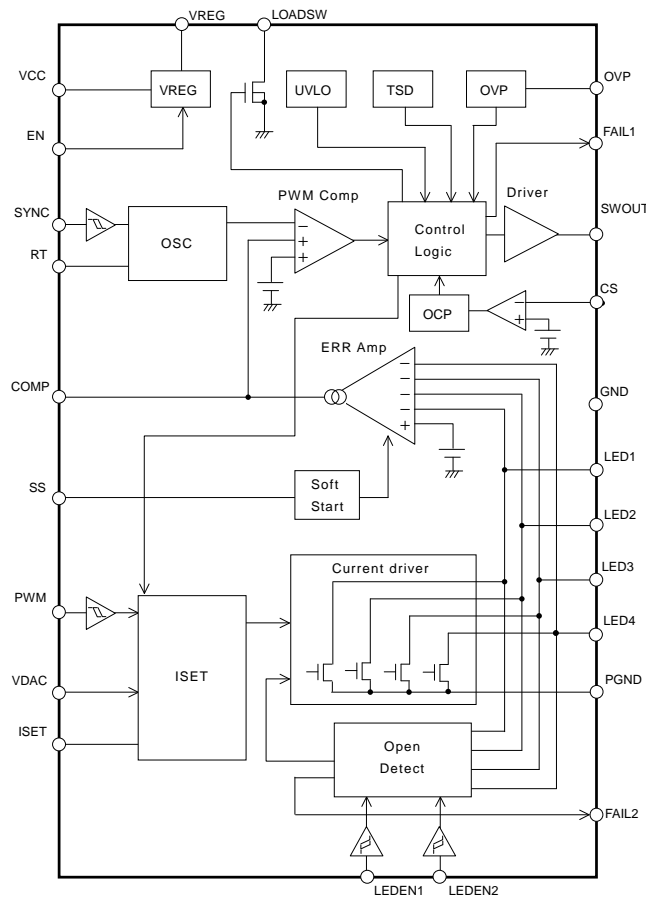
●Pin No, Pin Name, Function

Pin No	Pin Name	Function	Pin No	Pin Name	Function
1	Vcc	Power supply	15	LED3	LED output（Open Drain）
2	LOADSW	FET pin for load sw（Open Drain）	16	–	N.C
3	FAIL1	Fail signal output（Open Drain）	17	LED4	LED output（Open Drain）
4	VREG	Internal voltage regulator	18	–	N.C.
5	PWM	PWM adjustment input	19	–	N.C.
6	SYNC	External synchronizing input	20	FAIL2	Fail signal output (Open det : Open Drain)
7	GND	Ground pin	21	PGND	LED output GND pin
8	VDAC	DC flexible input	22	CS	DC/DC output current detection pin
9	ISET	LED output current set resistor	23	SWOUT	DC/DC SW output pin
10	LEDEN1	LED output enable pin1	24	EN	Enable pin
11	LEDEN2	LED output enable pin2	25	OVP	OVP pin over voltage detection pin
12	LED1	LED output（Open Drain）	26	RT	Frequency set resistor
13	–	N.C.	27	SS	Softstart pin
14	LED2	LED output（Open Drain）	28	COMP	Error amp output

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● Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered.
A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Reverse connection of a power supply connector

If the connector of power is wrong connected, it may result in IC breakage. In order to prevent the breakage from the wrong connection, the diode should be connected between external power and the power terminal of IC as protection solution.

(3) Power supply and ground lines.

Fluctuating voltage on the power supply and ground lines may damage the device. Be sure to connect a bypass filter capacitor as close as possible to the IC between the power supply and ground pins. Check that the selected capacitance will not have an adverse influence on any characteristics, such as a drop in the electrolytic capacitor value that can occur at low temperatures.

(4) GND potential

Ensure a minimum GND pin potential in all operating conditions.

(5) Setting of heat

Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards.Improper mounting may result in damage to the IC. Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage.

(7) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) Thermal shutdown circuit(TSD)

This IC built-in a Thermal shutdown circuit (TSD circuit). If Chip temperature becomes 175℃(TYP.), make the output an Open state. Eventually, warmly clearing the circuit is decided by the condition of whether the heat excesses over the assigned limit, resulting the cutoff of the circuit of IC, and not by the purpose of preventing and ensuring the IC. Therefore, the warm switch-off should not be applied in the premise of continuous employing and operation after the circuit is switched on.

(9) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress.
Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process

(10) IC terminal input

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when a resistor and transistor are connected to pins. (See the chart below.)

○ the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
○ Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input pins.
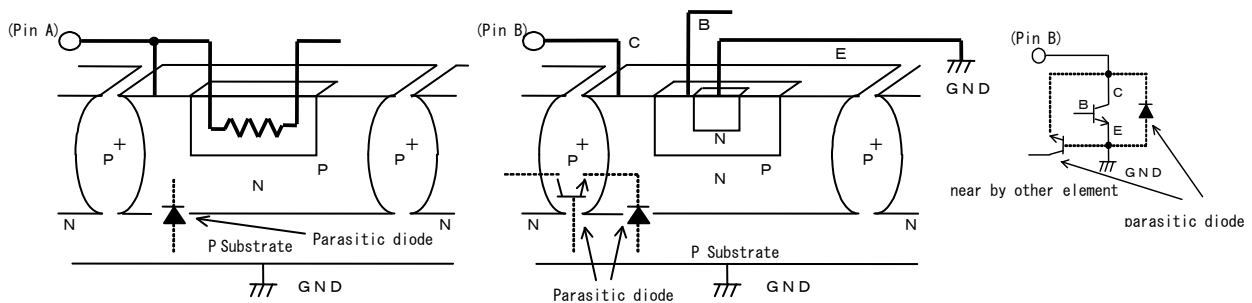

Fig of chart of Parasitic diode

(11) Ground wiring patterns

When using both small signal and large current GND patterns,it is recommended to isolate the two ground patterns,placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

(12) LED output terminal

Don't connect Capacitor to LED output terminal (Pin : 12,14,15,17), as doing so may cause LED short detection to malfunction.

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