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Si4x6x-B1B and Si4438-B1C Errata

This document describes the known errata items for EZRadioPRO Si4x6x-B1B-FM and Si4438-B1C-FM products.

Errata Status Summary

Issue	Workaround Available	Fix Identified for Future Revision
If configured to skip sync and preamble on transmit, the TX data from the FIFO is corrupted	Yes	Yes
When the CAL timer and Wakeup timer fire at the same time, the Wakeup timer function is skipped	Yes	Yes
CHANGE_STATE to TX from TX is an invalid state transition	This is an invalid state transition	N/A
TX packet abort does not reset the packet handler	Yes	Yes
Packet re-transmit does not function as expected	Yes	Yes
SPI active to Ready state without any SPI activity is not supported	Yes	Yes
Non-zero BER in Low Power mode at strong signal levels	FW Patch available	Yes
RSSI jump interrupt API not supported	No	Yes
RSSI status is not reset upon START_RX	Yes	Yes
Variable packet length cannot be zero	Yes	Yes
Ramp waveform of external PA ramp signal on TXRAMP pin is not correct.	No	Yes
Preamble detect signal for non-standard preambles is incorrect on the GPIO	No	Yes
For non-standard preambles, the modem can get stuck in low gear mode if gear switch is set to preamble	Yes	Yes

Issue	Workaround Available	Fix Identified for Future Revision
detection and sync word detection fails		
If the first received packet has a CRC error, subsequent packets will report a spurious command error	Yes	Yes
Use of TCXO with low Vdd supply may cause a CTS failure	FW Patch available	Yes
FIFO_INFO command does not update TX_FIFO_ALMOST_EMPTY status properly	Yes	Yes
FIFO threshold setting limitations	Yes	Yes

Errata Details

If configured to skip sync and preamble on transmit, the TX data from the FIFO is corrupted

Description:

If preamble and sync word are excluded from the transmitted data (PREMABLE_TX_LENGTH = 0 and SYNC_CONFIG: SKIP_TX = 1) the data from the FIFO is not transmitted correctly.

Impact:

There will be some number of missed bytes at the beginning of the packet, and some number of repeated bytes at the end of the packet.

Workaround:

Set PKT_FIELD_1_CRC_CONFIG: CRC_START to 1. This will trigger the packet handler and result in transmitting the correct data, while still not sending a CRC unless enabled in a FIELD configuration. A fix has been identified and will be included in a future release.

When the CAL timer and Wakeup timer fire at the same time, the Wakeup timer function is skipped

Description:

If the Wakeup timer and calibration timer intervals are chosen such that they will occur at the same time, the Wakeup timer function will not occur.

Impact:

When the Wakeup timer and calibration timer intervals coincide exactly, the Wakeup timer function will not occur. This will impact functionality that relies on the Wakeup timer under these specific conditions.

Workaround:

Configure the Wakeup timer and CAL timer to separate intervals. The CAL timer will first expire at half its programmed interval and at every programmed interval afterwards. The Wakeup timer always expires on its programmed interval after it is enabled. These intervals should be configured such that they never align. Alternatively, the RC calibration can be performed on Wakeup timer intervals as configured using GLOBAL_WUT_CAL API. A fix has been identified and will be included in a future release.

CHANGE_STATE to TX from TX is an invalid state transition

Description:

This is an invalid state change for the device. However, if the chip is currently in TX state and a CHANGE_STATE to TX or START_TX command is issued, the chip will stop responding. (CTS will remain low until the chip is reset).

Impact:

If attempting this invalid state transition, the host will not be able to issue subsequent commands to the device without resetting the device first. The device can be reset via the shutdown pin or by power cycling the Vdd supply to the device.

Workaround:

Avoid going from TX state to TX state directly. If the chip is in TX state, exit to some other state before starting TX again.

TX packet abort does not reset the packet handler

Description:

When a packet is aborted before it has completed transmitting by issuing a CHANGE_STATE out of TX state, the next transmission will continue where the previous packet stopped. For example, if START_TX is issued with TX_LEN = 700, then the packet is aborted after 300 bytes have been sent, the next TX will not send preamble and sync and will attempt to send 400 bytes.

Impact:

The second packet will have invalid information if the first packet is aborted during transmission with a change state out of TX state. This does not impact direct mode operation of the device.

Workaround:

To abort TX, always use CHANGE_STATE to SLEEP mode. Once in sleep mode, the device can change state to any other state properly. A fix has been identified and will be included in a future release.

Packet re-transmit does not function as expected

Description:

For packet re-transmission, user has to set the re-transmit bit to 1 in the very first packet transmitted. In the last transmission, user should set the bit to 0.

Impact:

If the first transmission has the re-transmit bit set to 0, re-transmission will not occur.

Workaround:

Set the re-transmit bit to 1 for the very first transmission. A fix has been identified and will be included in a future release.

SPI active to Ready state without any SPI activity is not supported

Description:

If the chip transitions from SPI active state to Ready state, there must be some SPI activity when leaving the SPI active state. This is not a common condition but can occur in a case where the user sets the device to SPI active state and the Wakeup timer to TX or RX a packet on timer expiry. This could also occur if the user goes from SPI active to Ready state and polls CTS on a GPIO instead of the SPI interface.

Impact:

The device cannot go from SPI active to Ready state without SPI activity.

Workaround:

Ensure there is SPI activity when going from SPI active to Ready state. A fix has been identified and will be included in a future release.

Non-zero BER in Low Power mode at strong signal levels

Description:

If the transceiver is in low power mode (default is high performance mode), there is a chance of non-zero BER at very strong signal levels (e.g. 1% BER at > -12 dBm).

Impact:

No impact in high performance mode which is the default setting. Non-zero BER (~1%) will be seen at strong signal levels.

Workaround:

None. A firmware patch is available on request and a fix has been identified and will be included in a future release.

RSSI jump interrupt API not supported

Description:

The RSSI jump interrupt indicates when there is a sudden change in RSSI. This feature is not supported in revision Si4x6x-B1B and Si4438-B1C.

Impact:

RSSI jump interrupt functionality is not supported in this revision.

Workaround:

None. A fix has been identified and will be included in a future release.

RSSI status is not reset upon START_RX

Description:

Transitioning out of RX state and then going back to RX will not result in automatically resetting RSSI status. ‘RSSI pending’ indicates if sometime during RX the current RSSI ever went above the threshold, while ‘RSSI status' indicates if the current RSSI is above the threshold at the moment.

Impact:

The chip will not be able to generate an RSSI interrupt more than once without leaving RX state and manually clearing the RSSI interrupt.

Workaround:

User has to manually clear the RSSI interrupt with a GET_INT_STATUS command outside of RX state. A fix has been identified and will be included in a future release.

Variable packet length cannot be zero

Description:

If the variable packet length field is set to zero, the device will stay in RX state and preamble and sync detect signals will remain high (e.g: detected in noise).

Impact:

Variable packet length of zero will cause the device to remain in RX state.

Workaround:

Set the variable packet length to a non-zero value. A fix has been identified and will be included in a future release.

Ramp waveform of external PA ramp signal on TXRAMP pin is not smooth

Description:

The TXRAMP pin is intended to ramp external PAs when higher TX power is desired. The waveform is not smooth and could cause transient spectral splatter that impacts certain regulatory requirements.

Impact:

Potentially impacts certain regulatory requirements due to transient spectral splatter.

Workaround:

Add RC filtering on the board to smoothen the TXRAMP signal. A fix has been identified and will be included in a future release.

Preamble detect signal for non-standard preambles is incorrect on the GPIO

Description:

Preamble detection for non-standard (non 1010) patterns is not indicated correctly on GPIOs.

Impact:

The host cannot use the GPIO to indicate detection of a non-standard preamble.

Workaround:

None. A fix has been identified and will be included in a future release.

For non-standard preambles, the modem may remain in low gear mode if gear switch is set to preamble detection and sync word detection fails

Description:

The modem can switch gears (signal acquisition speed) based on preamble detection. If the sync word is not detected after preamble detection, the modem will remain in low gear mode. This is only observed when using non-standard preambles.

Impact:

Less than 1dB degradation in sensitivity as the modem will remain in low gear mode.

Workaround:

Set the gear switch condition to sync word detection instead of preamble detection. A fix has been identified and will be included in a future release.

If the first received packet has a CRC error, subsequent packets will report an error

Description:

If the first received packet has a CRC error, the next packet will raise a CMD_ERR interrupt in the middle of the packet.

Impact:

The device is still functional but a spurious CMD_ERR interrupt will occur.

Workaround:

After a packet with CRC error is received, go to sleep state before going back to receive state. A fix has been identified and will be included in a future release.

Use of TCXO with low Vdd supply may cause a CTS failure

Description:

In high performance mode, use of TCXO as clock source with a supply voltage of less than 2.3V may cause CTS failures if there are state transitions. This occurs at specific temperatures within the operating temperature range and varies from chip to chip.

Impact:

Without a CTS response, the host MCU will be unable to send further commands to the transceiver.

Workaround:

A firmware patch is available on request and a fix has been identified which will be included in a future release. Workarounds include increasing supply voltage to above 2.3V when using a TCXO, switching to a XTAL clock source or using the device in low power (LP) mode.

FIFO_INFO command does not update TX_FIFO_ALMOST_EMPTY status properly

Description:

If the TX FIFO is reset by the FIFO_INFO command, the chip does not update the TX_FIFO_ALMOST_EMPTY status bit correctly. It gets updated only by the next TX FIFO fill that causes the TX_FIFO_ALMOST_EMPTY interrupt to occur later than expected.

Impact:

TX_FIFO_ALMOST_EMPTY interrupt occurs later than expected.

Workaround:

Write one dummy byte into the TX_FIFO to fire the TX_FIFO_ALMOST_EMPTY interrupt and reset the TX_FIFO again. A fix has been identified and will be included in the next revision of the device.

FIFO Threshold Limitations

Description:

Threshold of TX_FIFO_ALMOST_EMPTY interrupt can only be set to as high as 58 bytes for reliable interrupt generation when the threshold is reached. If the payload length of the transmitted packet is less than 7 bytes, the user can rely on the PACKET_SENT interrupt which indicates the end of packet transmission.

Threshold of RX_FIFO_ALMOST_FULL interrupt can only be set to as low as 12 bytes for reliable interrupt generation when the threshold is reached. If the payload length of the received packet is less than 12 bytes, the user can rely on the PACKET_RX interrupt which indicates the end of packet.

Impact:

User should not rely on FIFO threshold interrupts for greater than 58 bytes on the TX side and less than 12 bytes on the RX side.

Workaround:

Rely on PACKET_SENT and PACKET_RX interrupts for very small payload lengths as described above. A fix has been identified and will be included in the next revision of the device.