N- and P-Channel 30V (D-S) Power MOSFET

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

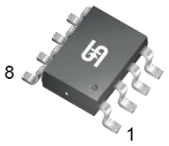
APPLICATIONS

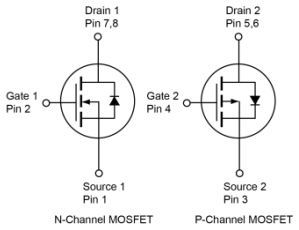
- DC-DC Converters
- Power Routing
- Motor Drives

KEY PERFORMANCE PARAMETERS				
PARAMETER		**TYPE**	**VALUE**	**UNIT**
V_{DS}		N-ch	30	V
		P-ch	-30	
$R_{DS(on)}$ (max)	V_{GS} = 10V	N-ch	16	mΩ
	V_{GS} = 4.5V		20	
	V_{GS} = -10V	P-ch	24	
	V_{GS} = -4.5V		37	
Q_g		N-ch	7	nC
		P-ch	11	

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)					
PARAMETER		**SYMBOL**	**N-ch**	**P-ch**	**UNIT**
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±25	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	15	13	A
	T_A = 25°C		8	7	
Pulsed Drain Current		I_{DM}	60	52	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	12	18	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	21.6	48.6	mJ
Total Power Dissipation	T_C = 25°C	P_D	6	6	W
	T_C = 125°C		1.2	1.2	
Total Power Dissipation	T_A = 25°C	P_D	1.6	1.6	W
	T_A = 125°C		0.3	0.3	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	21	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	78	

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	N-ch	30	--	--	V
	V_{GS} = 0V, I_D = -250μA		P-ch	-30	--	--	
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	N-ch	1	1.4	2.5	V
	V_{GS} = V_{DS}, I_D = -250μA		P-ch	-1	-1.7	-2.5	
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	N-ch	--	--	±100	nA
	V_{GS} = ±25V, V_{DS} = 0V		P-ch	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 30V	I_{DSS}	N-ch	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 30V T_J = 125°C			--	--	100	
	V_{GS} = 0V, V_{DS} = -30V		P-ch	--	--	-1	
	V_{GS} = 0V, V_{DS} = -30V T_J = 125°C			--	--	-100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 8A	$R_{DS(on)}$	N-ch	--	10	16	mΩ
	V_{GS} = 4.5V, I_D = 8A			--	13	20	
	V_{GS} = -10V, I_D = -7A		P-ch	--	18	24	
	V_{GS} = -4.5V, I_D = -7A			--	30	37	
Forward Transconductance (Note 3)	V_{DS} = 5V, I_D = 8A	g_{fs}	N-ch	--	26	--	S
	V_{DS} = -5V, I_D = -7A		P-ch	--	16	--	
Dynamic (Note 4)							
Total Gate Charge	N-ch V_{DS} = 15V, I_D = 8A P-ch V_{DS} = -15V, I_D = -7A	$Q_{g(VGS=10V)}$	N-ch	--	14	--	nC
			P-ch	--	21.5	--	
Total Gate Charge		$Q_{g(VGS=4.5V)}$	N-ch	--	7	--	
			P-ch	--	11	--	
Gate-Source Charge		Q_{gs}	N-ch	--	1.7	--	
			P-ch	--	3.4	--	
Gate-Drain Charge		Q_{gd}	N-ch	--	3.7	--	
			P-ch	--	5.3	--	
Input Capacitance	N-ch V_{GS} = 0V, V_{DS} = 15V f = 1.0MHz P-ch V_{GS} = 0V, V_{DS} = -15V f = 1.0MHz	C_{iss}	N-ch	--	646	--	pF
			P-ch	--	1089	--	
Output Capacitance		C_{oss}	N-ch	--	108	--	
			P-ch	--	190	--	
Reverse Transfer Capacitance		C_{rss}	N-ch	--	70	--	
			P-ch	--	119	--	
Gate Resistance	f = 1.0MHz	R_g	N-ch	0.9	3	6	Ω
			P-ch	3.6	12	24	

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Switching (Note 4)							
Turn-On Delay Time	N-ch V_{GS} = 10V, V_{DS} = 15V, I_D = 8A, R_G = 2Ω P-ch V_{GS} = -10V, V_{DS} = -15V, I_D = -7A, R_G = 2Ω	$t_{d(on)}$	N-ch	--	5.4	--	ns
			P-ch	--	6.2	--	
Turn-On Rise Time		t_r	N-ch	--	41.3	--	
			P-ch	--	40.4	--	
Turn-Off Delay Time		$t_{d(off)}$	N-ch	--	18	--	
			P-ch	--	45.4	--	
Turn-Off Fall Time		t_f	N-ch	--	5.6	--	
			P-ch	--	45.4	--	
Source-Drain Diode							
Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 8A	V_{SD}	N-ch	--	--	1	V
	V_{GS} = 0V, I_S = -7A		P-ch	--	--	-1	
Reverse Recovery Time	N-ch I_S = 8A, dI/dt = 100A/μs P-ch I_S = -7A, dI/dt = 100A/μs	t_{rr}	N-ch	--	14	--	ns
			P-ch	--	32	--	
Reverse Recovery Charge		Q_{rr}	N-ch	--	4	--	nC
			P-ch	--	10	--	

Notes:

1. Silicon limited current only.
2. N-ch : L = 0.3mH, V_{GS} = 10V, V_{DD} = 25V, R_G = 25Ω, I_{AS} = 12A, Starting T_J = 25°C
   P-ch : L = 0.3mH, V_{GS} = 10V, V_{DD} = 25V, R_G = 25Ω, I_{AS} = 18A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

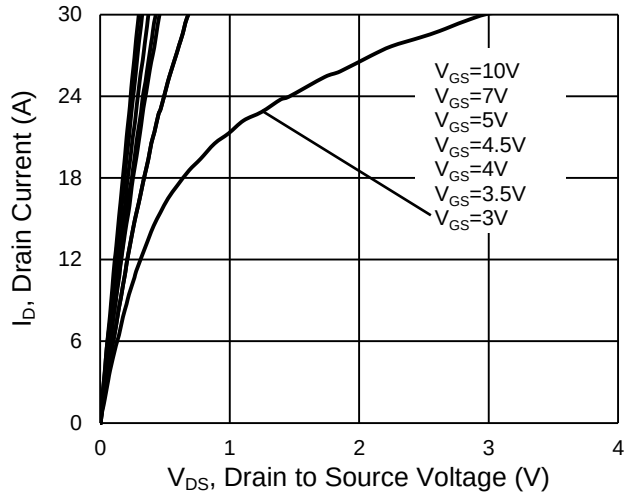
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM8568CS RLG	SOP-8	2,500pcs / 13” Reel

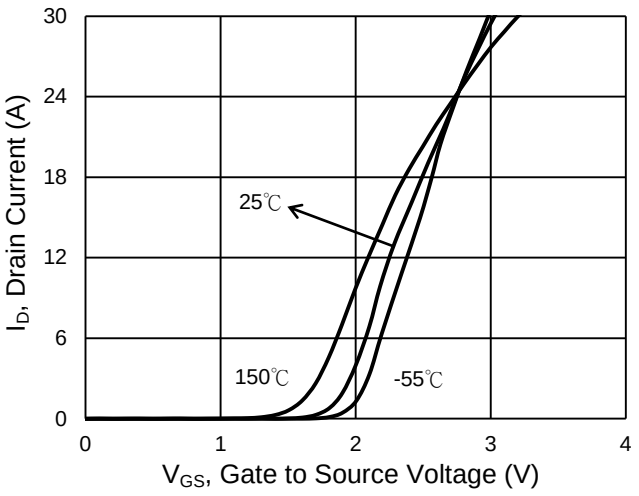
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

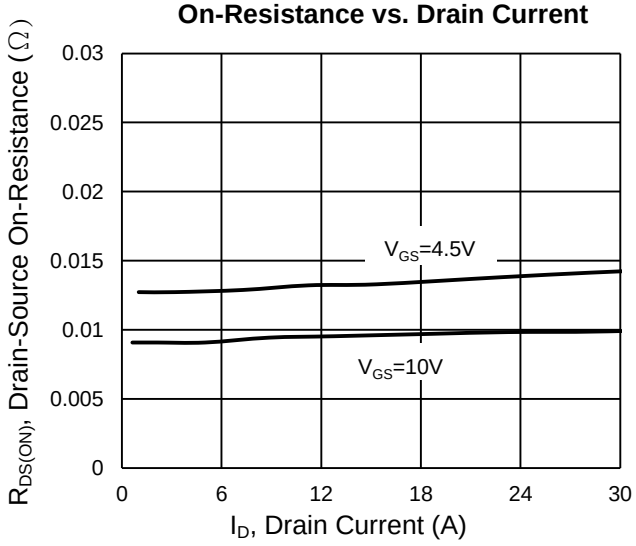
Output Characteristics



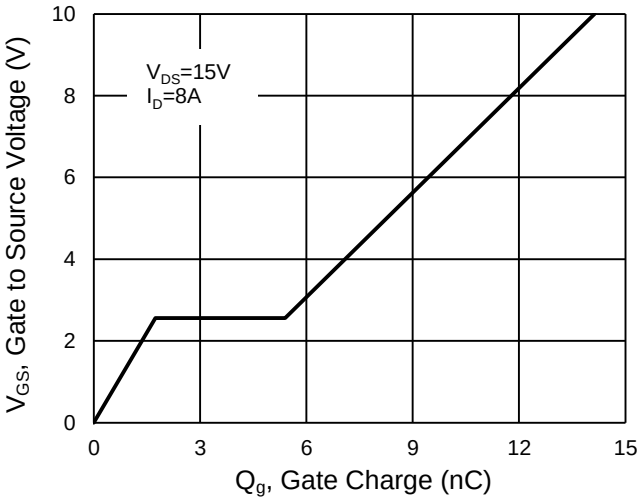
Transfer Characteristics



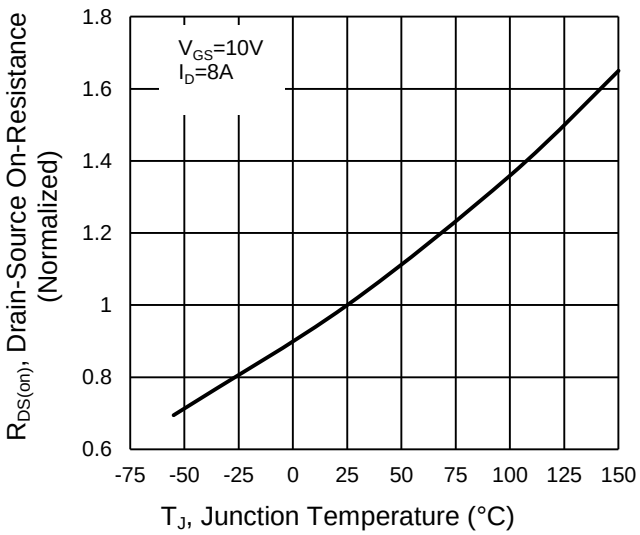
On-Resistance vs. Drain Current



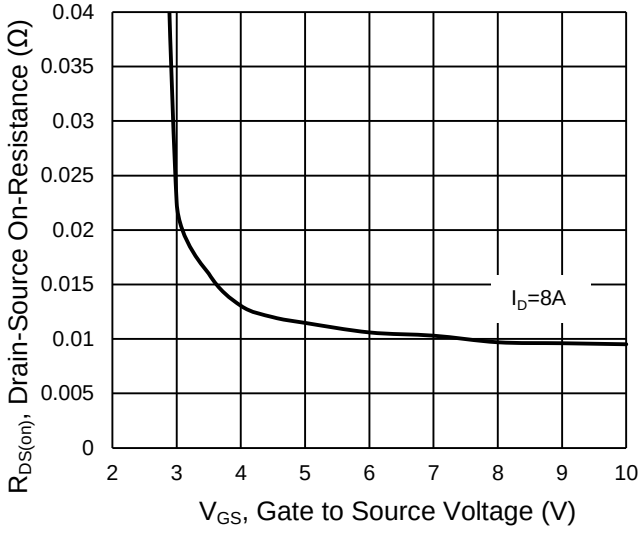
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



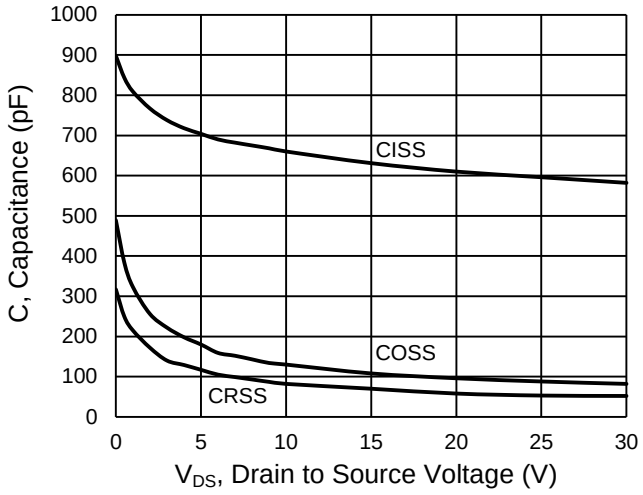
On-Resistance vs. Gate-Source Voltage



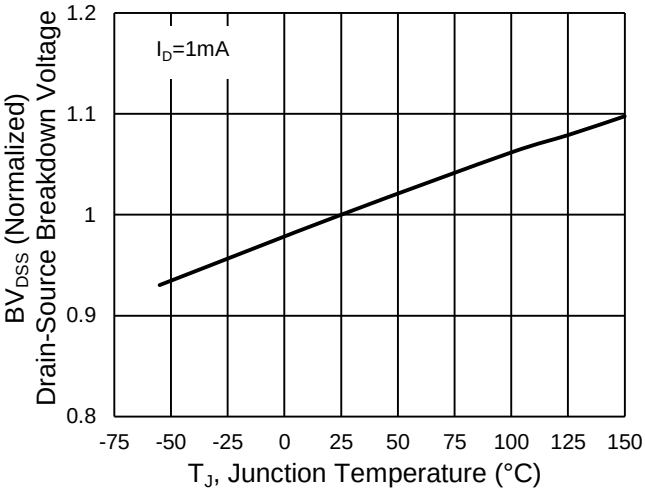
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

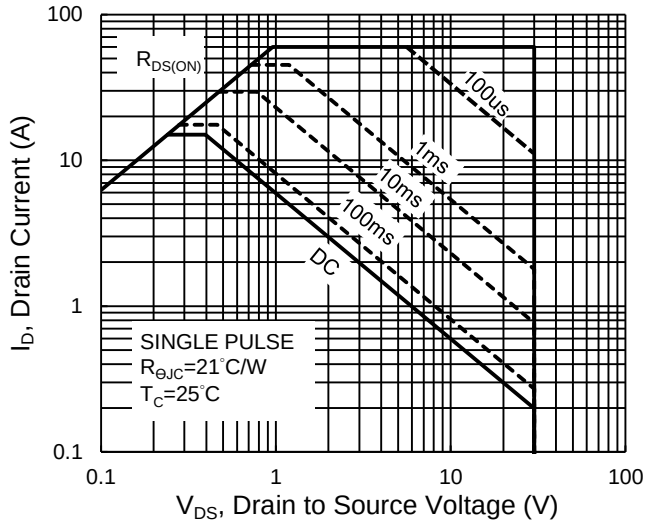
Capacitance vs. Drain-Source Voltage



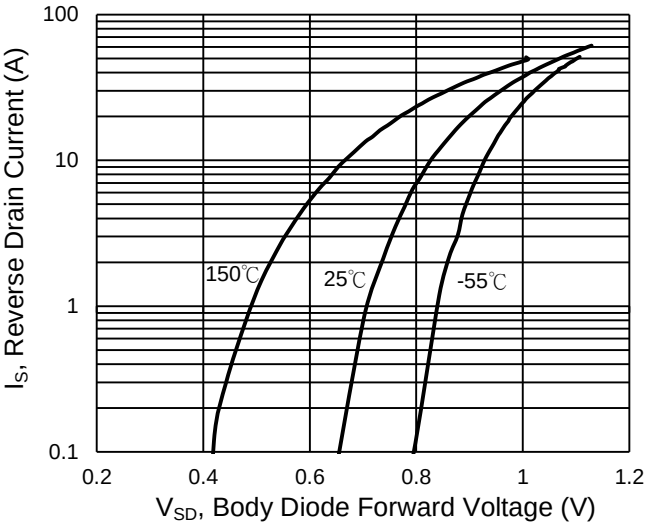
BV_{DSS} vs. Junction Temperature



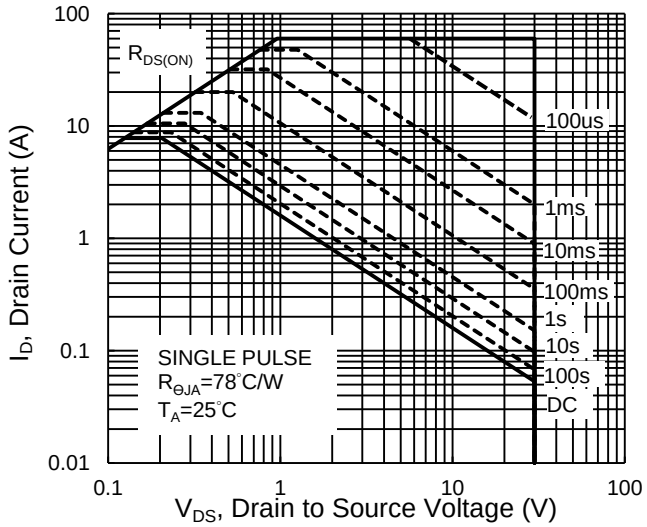
Maximum Safe Operating Area, Junction-to-Case



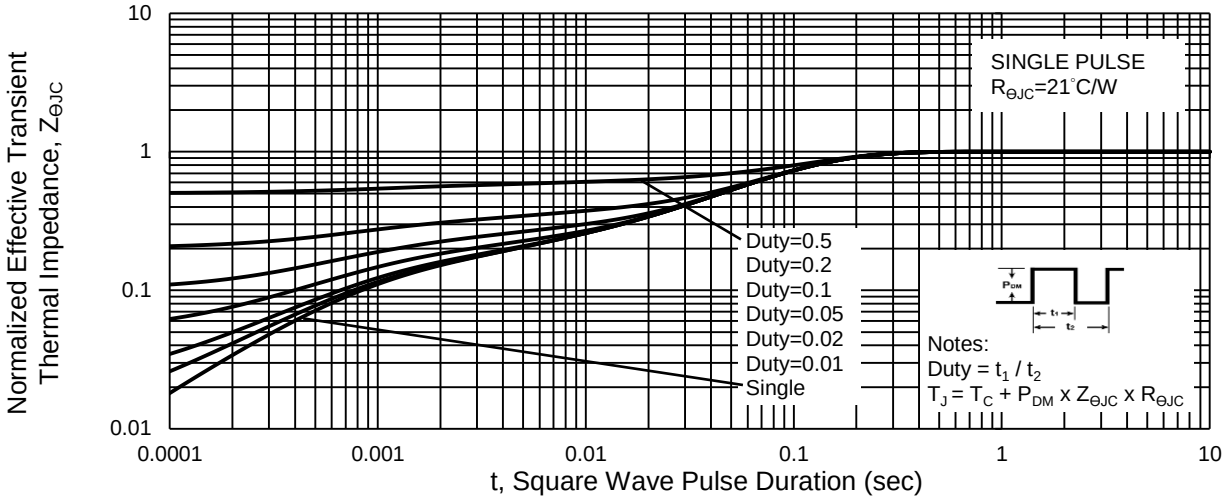
Source-Drain Diode Forward Current vs. Voltage



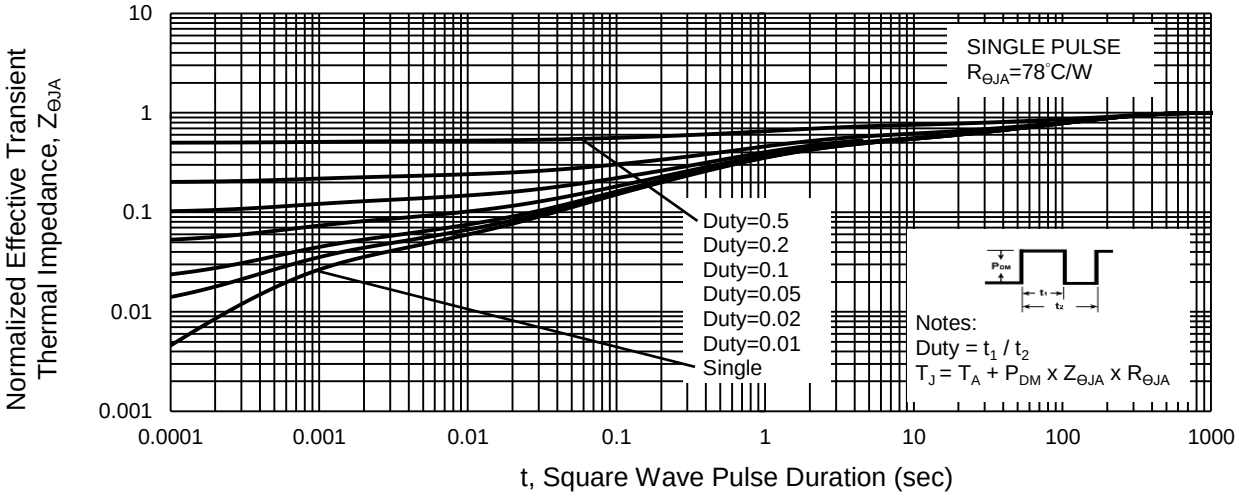
Maximum Safe Operating Area, Junction-to-Ambient



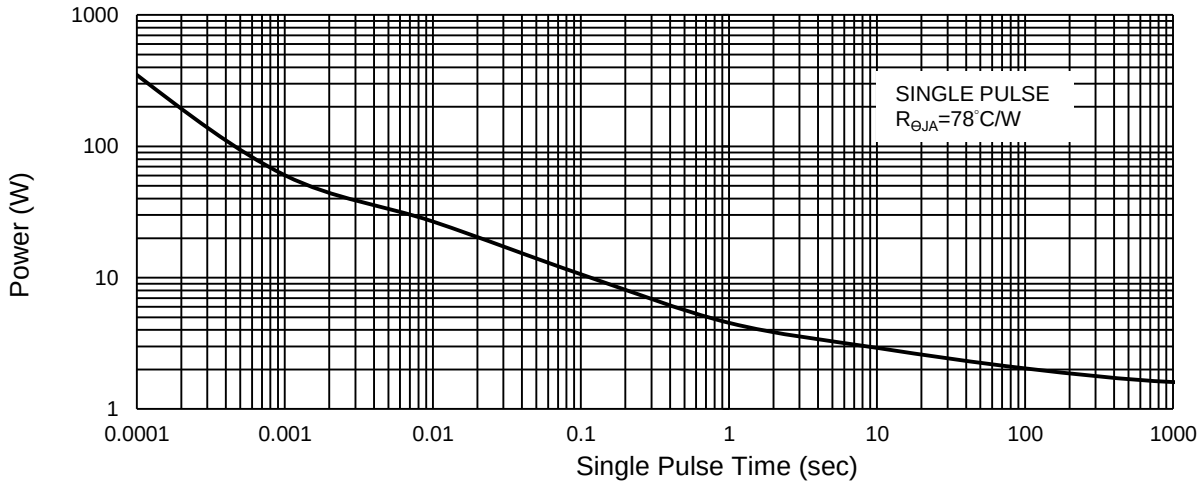
Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



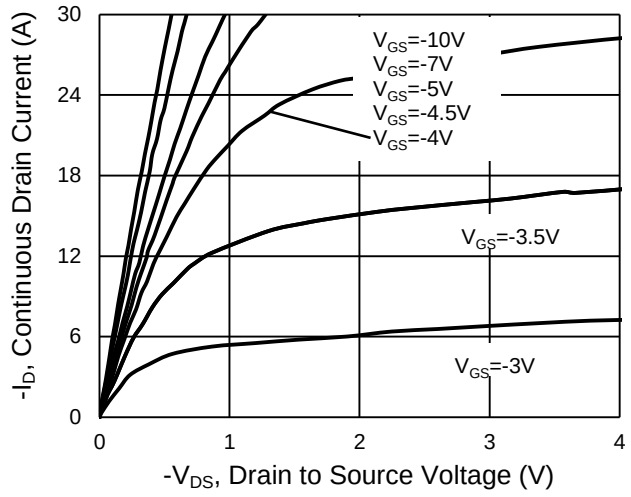
Single Pulse Maximum Power Dissipation, Junction-to-Ambient



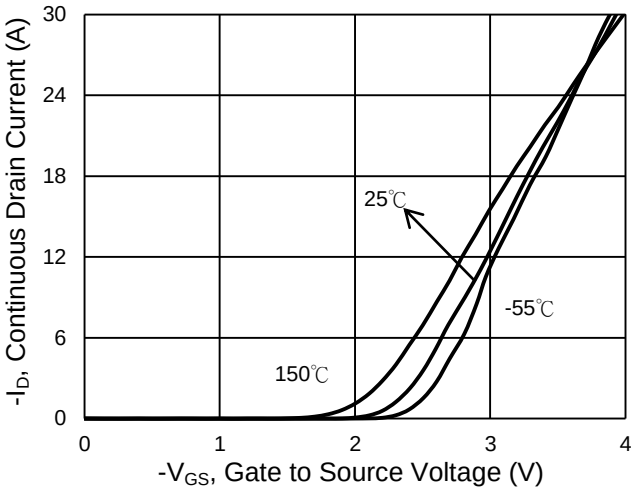
CHARACTERISTICS CURVES (P-Channel)

(T_A = 25°C unless otherwise noted)

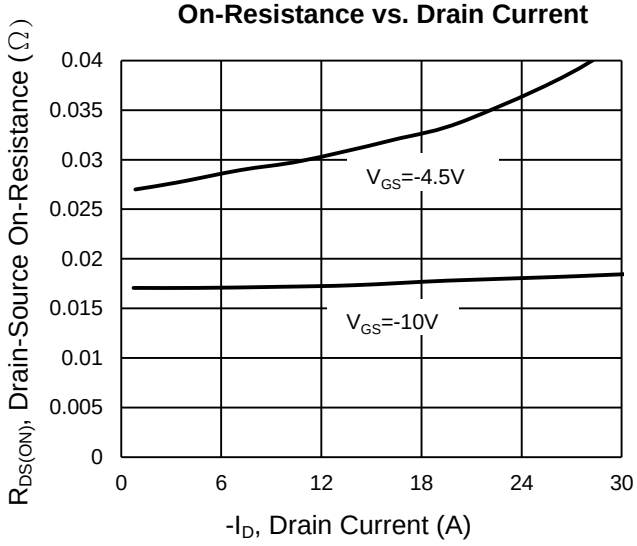
Output Characteristics



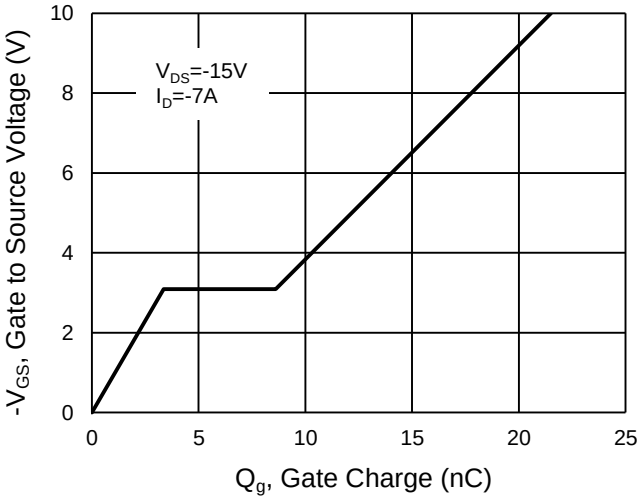
Transfer Characteristics



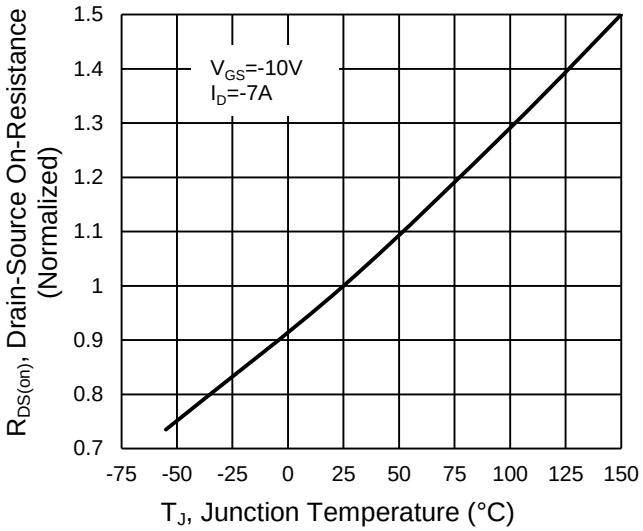
On-Resistance vs. Drain Current



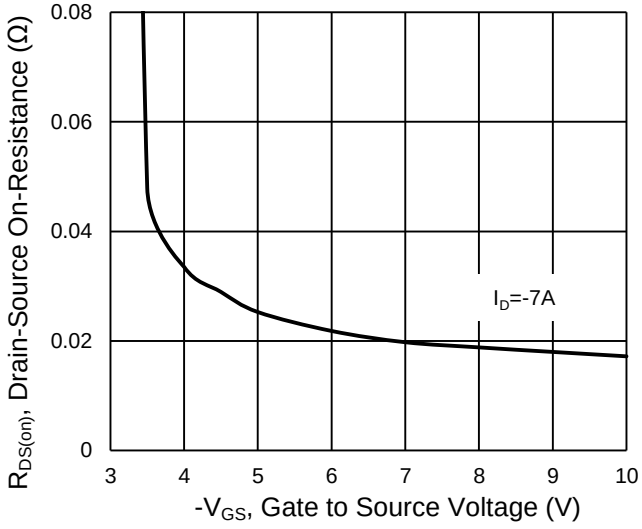
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



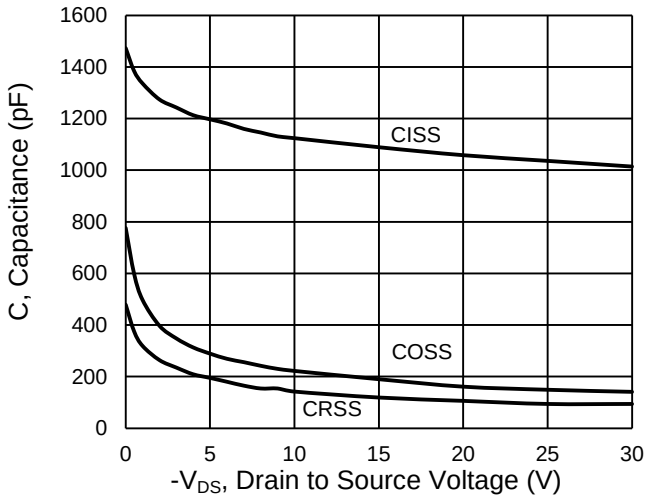
On-Resistance vs. Gate-Source Voltage



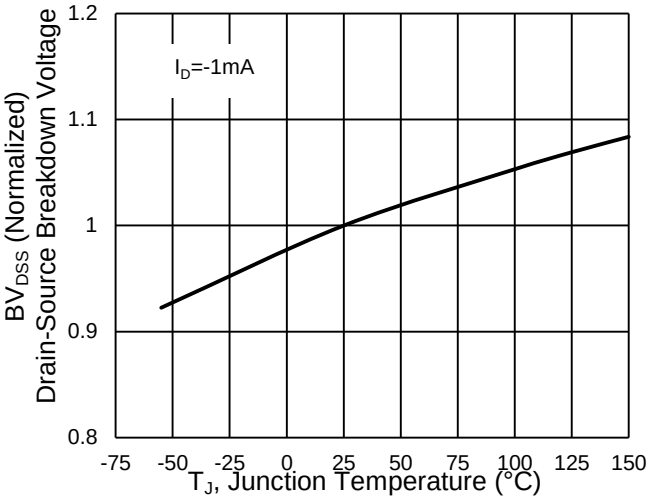
CHARACTERISTICS CURVES (P-Channel)

(T_A = 25°C unless otherwise noted)

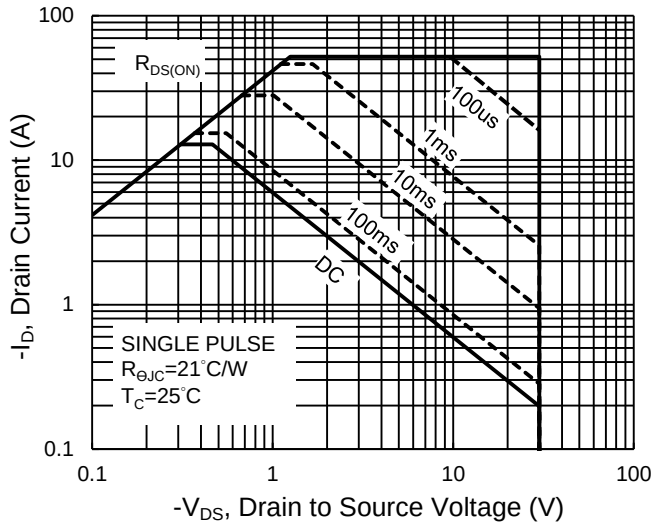
Capacitance vs. Drain-Source Voltage



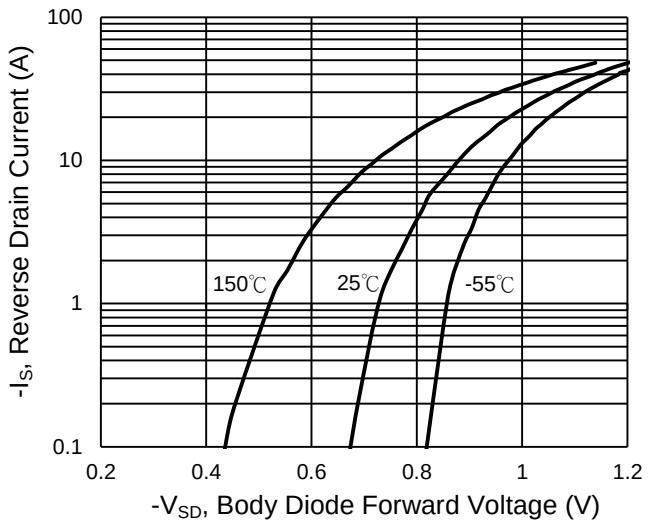
BV_{DSS} vs. Junction Temperature



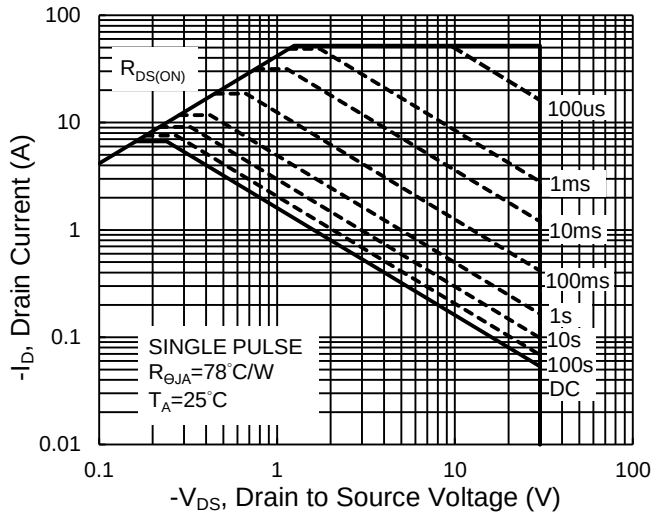
Maximum Safe Operating Area, Junction-to-Case



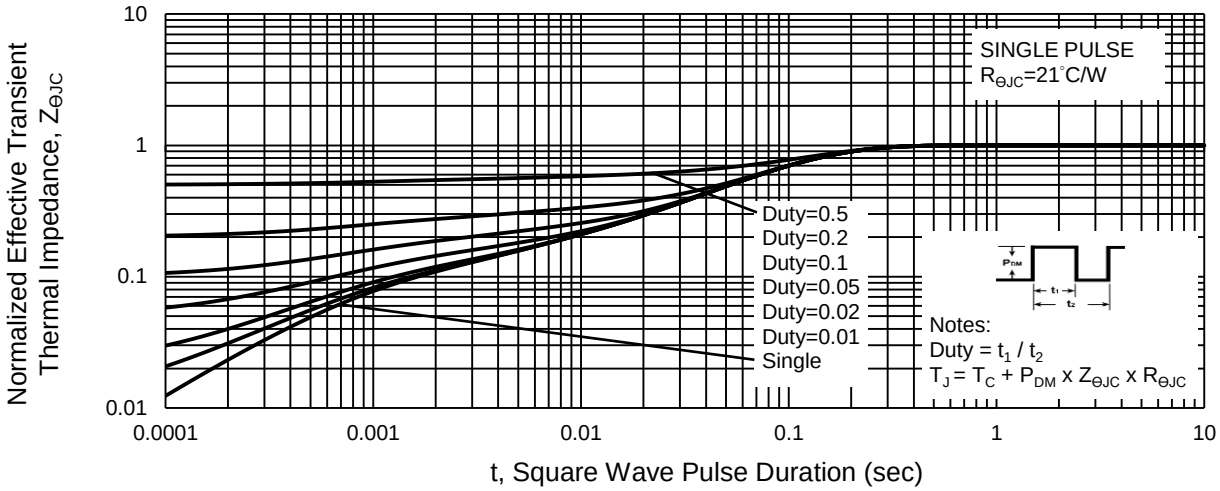
Source-Drain Diode Forward Current vs. Voltage



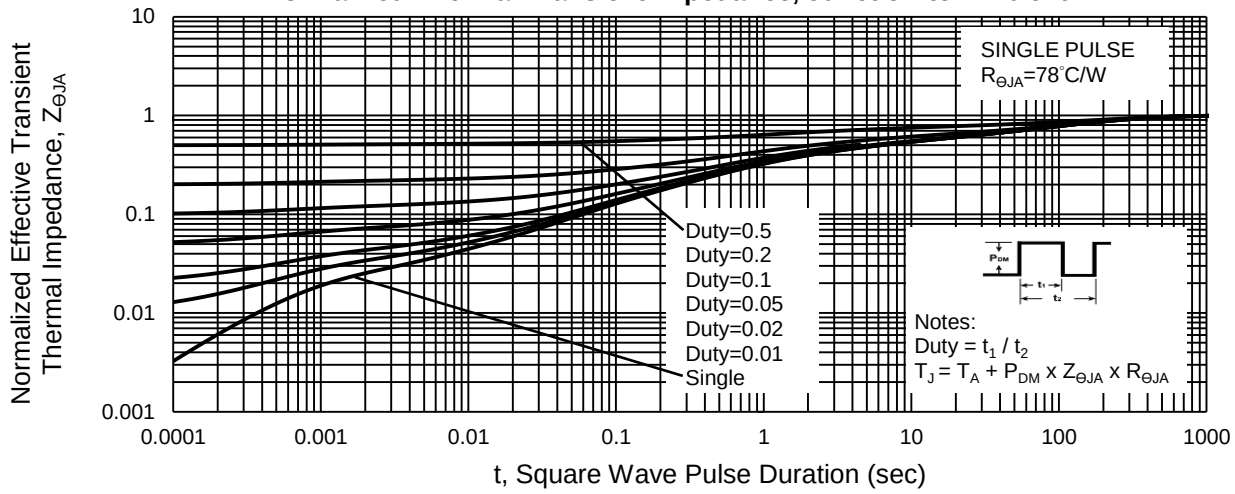
Maximum Safe Operating Area, Junction-to-Ambient



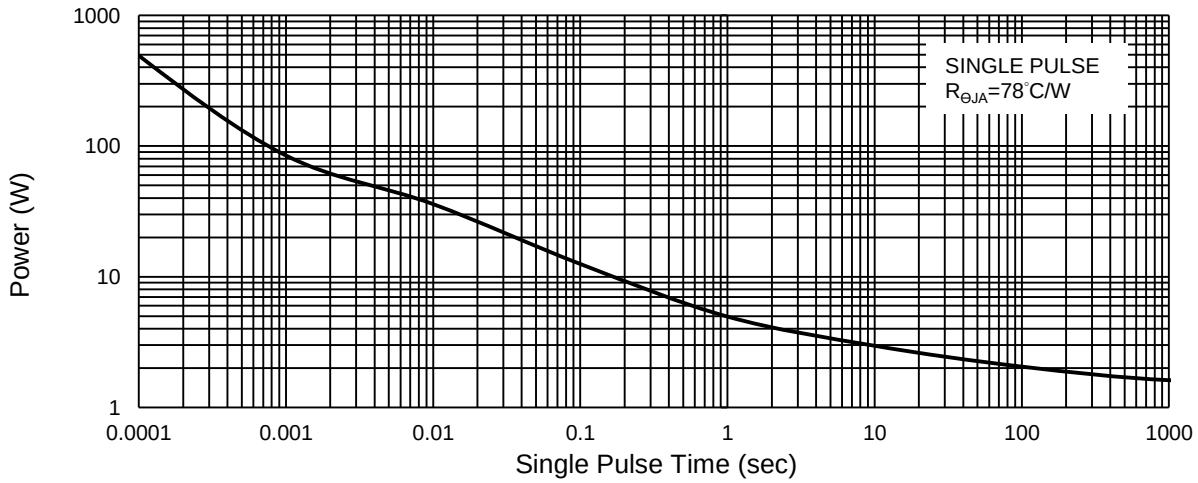
Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

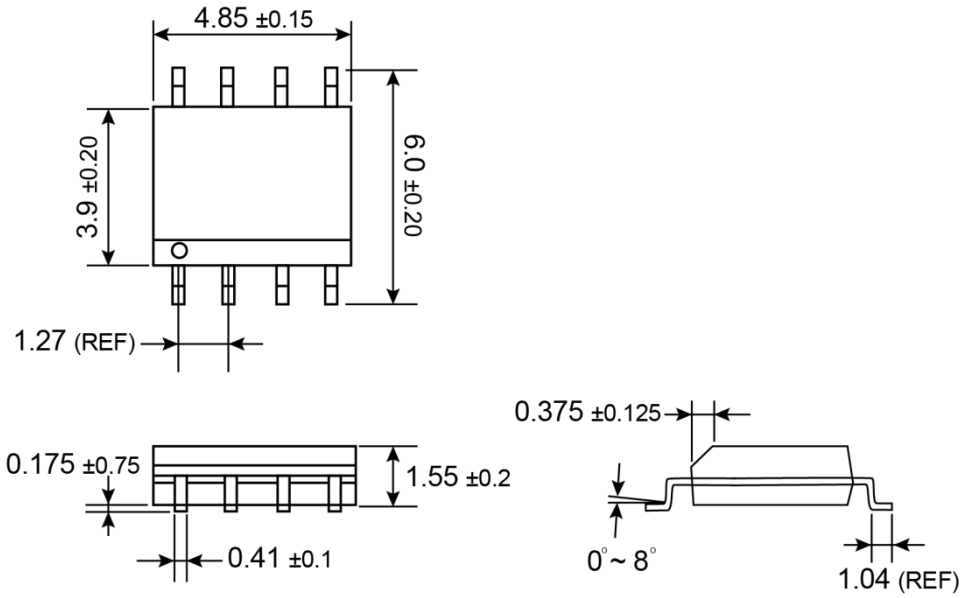


Single Pulse Maximum Power Dissipation, Junction-to-Ambient

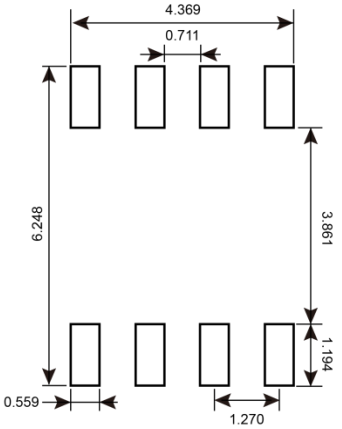


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

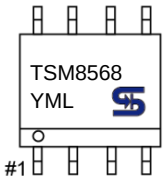
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code
M = Month Code

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

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