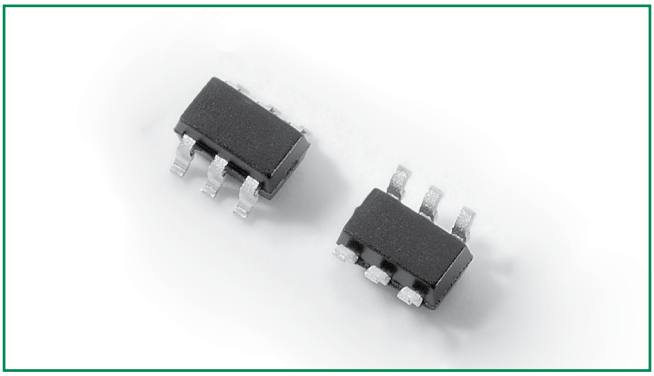
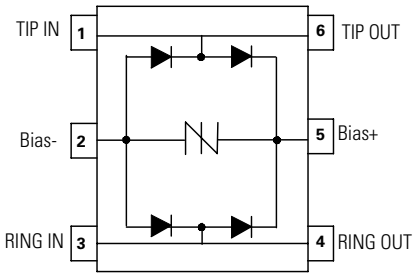
DSLP Biased Series - SOT23-6



Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation & Schematic Symbol



Description

This new DSLP Biased Series provides overvoltage protection for applications such as HD-SDI, HD-CVBS, VDSL2, ADSL2, ADSL2+, and G.fast with minimal effect on data signals. This silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications.

These components adopt the patent granted EpiSCR silicon crowbar technology and industry popular cost competitive SOT23-6 package with flow-through lead frame design.

There are various V_{DRM} options available in this series. This technology provides a better surge capability than traditional clamping silicon technology. This reduces the possibility of field failures caused by A.C. power fault and multiple transient surges or lightning without compromising the signal integrity particularly at high data rate.

Features & Benefits

- Compatible to VDSL2+ and G.fast (106MHz)
- Balanced voltage protection
- Superior surge capability of min 30Amp, typ 35Amp @ 8/20µS, typ 15 Amp @ 5/310µS
- Fast response time
- Wide variety V_{DRM} options for precise protection level needs
- Ultra low capacitance characteristic provides low insertion loss and less distortion particularly in higher data rate signals
- Low insertion loss
- RoHS Compliant
- Flow-though pin assignment and layout ideal for high data rate
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- ANSI C62.41
- IEC 61000-4-12
- IEC 61000-4-5 2nd edition, min 30A (t_P=8/20µs)
- IEC 61000-4-2 level 4
  - – 30kV (air discharge)
  - – 30kV (contact discharge)

Absolute Maximum Ratings between pin1 and pin 3, Ta= 25°C (Unless otherwise noted)

Part Number	Marking	Maximum Junction Temperature	Storage Temperature Range	I_{pp} 8/20µs	
		°C	°C	A min	A typ
DSLP0080T023G6RP	P08	150	-55 to 150	30 [1]	35 [1]
DSLP0120T023G6RP	P12	150	-55 to 150	30 [1]	35 [1]
DSLP0180T023G6RP	P18	150	-55 to 150	30 [1]	35 [1]
DSLP0240T023G6RP	P24	150	-55 to 150	30 [1]	35 [1]
DSLP0360T023G6RP	P36	150	-55 to 150	30 [1]	35 [1]

Notes:

1. The device must be in thermal equilibrium at 25°C

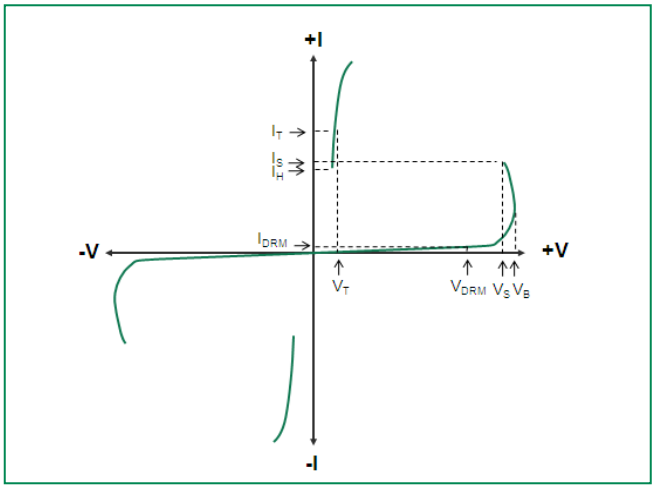
Revised: 09/12/16

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

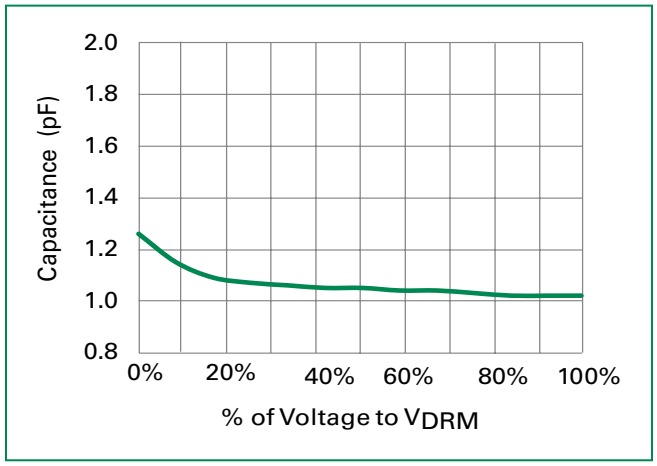
Electrical Characteristics between pin 1 and pin 3, Ta = 25°C

Part Number	Marking	V_{DRM} @I_{DRM}=100nA	I_R @V_{DRM}	V_S@100V/µs	I_H	I_S	Capacitance @f=1MHz,2V bias		Delta Co@ Line Bias = 1 V to V_{DRM}
		V min	pA typ	V max	mA typ	mA min	pF typ	pF max	pF max
DSLP0080T023G6RP	P08	8	300	18	40	10	1.3	2.5	0.4
DSLP0120T023G6RP	P12	12	300	22	40	10	1.3	2.5	0.4
DSLP0180T023G6RP	P18	18	300	28	40	10	1.3	2.5	0.4
DSLP0240T023G6RP	P24	24	300	34	40	10	1.3	2.5	0.4
DSLP0360T023G6RP	P36	36	300	48	40	10	1.3	2.5	0.4

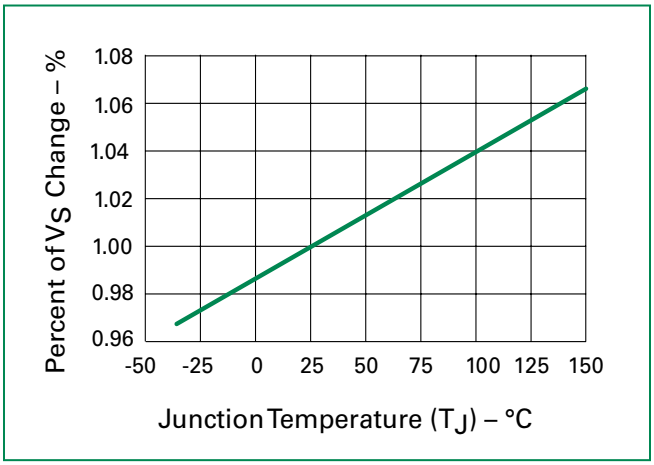
V-I: Characteristics



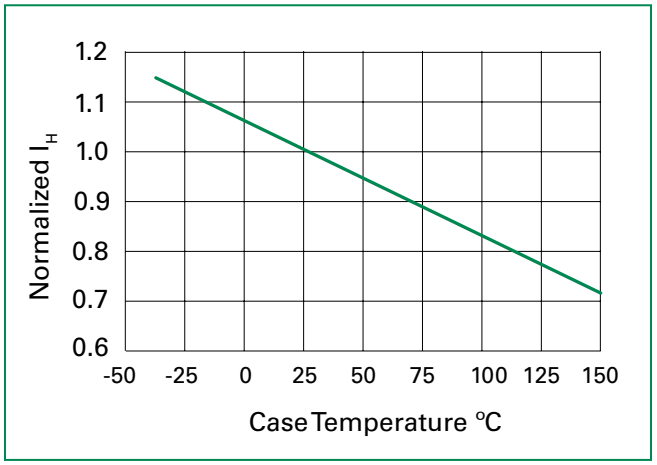
Typical capacitance against line voltage (without external bias)



Normalized V_S Change vs. Junction Temperature



Normalized Holding Current vs. Case Temperature



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SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Surge Ratings

Series	I_{PP}		
	8/20 [1] 1.2/50 [2]		5/310 [1] 10/700 [2]
	A min	A typ	A typ
G	30	35	15

Notes:

1 Current waveform in µs

2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- The component must be in thermal equilibrium at 25°C.

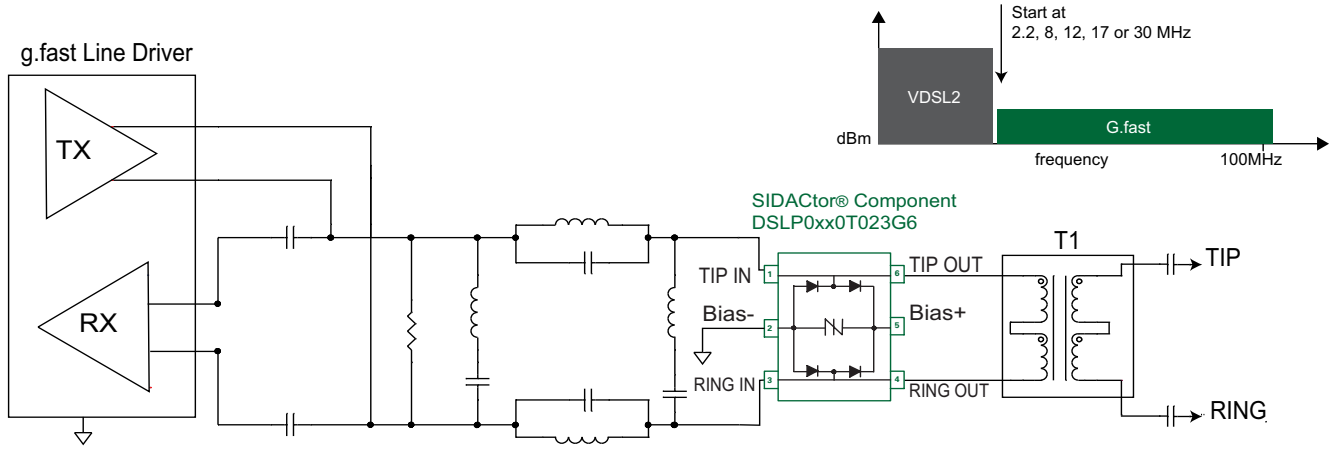
Thermal Information

Parameter	Value	Unit
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	260	°C

Application example - G.fas Protection

G.fast has a targeted data rate of 1Gbps over 100 m of single twisted pair (24 AWG/0.5 mm) cable using DSL-like technology.

This TDD (Time Division Duplex) signaling is a major difference from the existing FDD (Frequency Division Duplex) DSL signaling. G.fast bandwidth will extend up to 106 MHz (with the potential of going as high as 212 MHz) with the start frequency ranging from 2.2 MHz up to 30 MHz in an effort to avoid interference with existing xDSL services. G.fast may also employ "notching" where it suppresses carriers at specific individual frequencies to avoid clashing with local RF services.



About G.fast

The g.fast amplitude is very low as compared to existing xDSL services and thus the varying voltage across the SIDACtor® component is very low. This results in imperceptible capacitance variance of the over voltage protection (OVP) component; therefore the bias pins 2 & 5 may be left open in most applications. Rate and reach testing has shown an acceptable loss of less than 0.2dB with the DSLP0xx0T023G6RP component included at the tertiary position. Additionally, the flow-through layout of this component reduces the impedance mismatching "stub-effect" caused by non-"flow-through" PCB trace connections and provides for an easier PCB design. The small SOT23-6 footprint conserves valuable PCB real-estate space requriements.

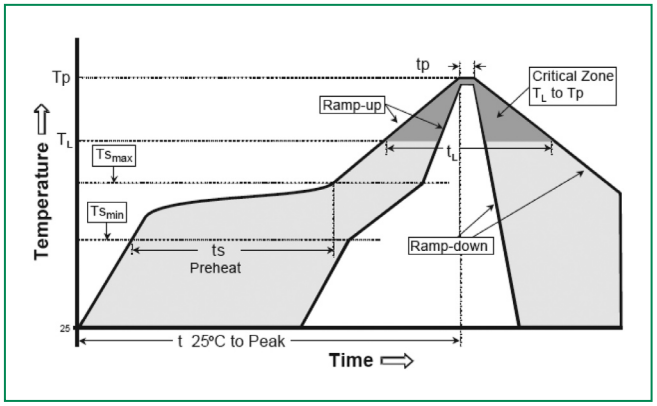
Since this interface is capacitively coupled, no fusing is required for power fault protection, however; selection of appropriately voltage rated capacitors must be considered regarding lightning exposure risks. The coupling transformer should have an isolation rating of at least 1.5kV 50/60Hz and consideration of its lightning response characteristics must also be considered. The I_{PP} 8/20 surge rating of this DSLP0xx0T023G6RP series is 30A minimally with a typical I_{PP} rating of 35A based on this waveshape. This should be sufficient for even the most severe exposure g.fast applications (including GR-1089 Issue 6 interbuilding requirements and ITU K20/21/45 Enhanced external line recommendations). The "Bias -" lead can be connected to the line driver ground with the "Bias + " lead left open so this solution provides both differential and common mode protection. Both "Bias -" and "Bias +" leads can be left floating for differential only protection and finally for capacitance variance sensitive applications, the "Bias -" and "Bias +" leads may have the appropriate polarity voltage (< V_{DRM}) applied to further minimize any negative capacitance effects.

The higher V_{DRM} components in this DSLP series can be considered for ADSL2, ADSL2+ and VDSL2 applications where the signal levels are much higher than the g.fast signals. The low off-state capacitance (2pF max) and the flow-through compatible SOT23-6 footprint properties of this series is also beneficial for these other xDSL applications.

Revised: 09/12/16

Soldering Parameters

Reflow Condition		Pb-Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		250(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		20-40 secs.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		260°C



Physical Specifications

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC MO-178
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte tine

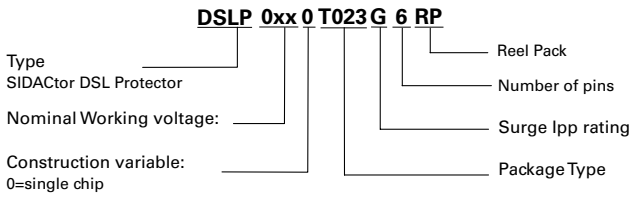
High Reliability Test Specification

Pre-condition (HTRB/ TC/ PCT/ H3TRB)	(1) Bake 24hrs @150°C (2)168hrs @85% RH and 85°C (3) I_R reflow,3 reflows, peak temperature of 260°C
HTRB	JESD 22-108 V_{CC} bias= 80%V_{DRM} & T_A=150°C, 1008hrs
Temperature Cycling	MIL-STD-883, Method 1010.8 Condition C -65°C to150°C, 1000 cycles
Pressure Cooker	JEDEC 22-A102 100%RH @121°C @15psi, 96hrs
Bias Humidity (H3TRB)	JESD 22-A101 Vcc bias (pin1to pin3)=V_{DRM} ,85%RH, 85°C , 1008 hours
RSH	JESD 22-A111 260°C ,10 secs.

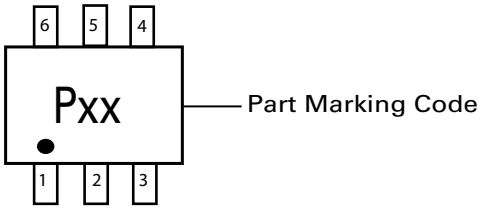
Packing Options

Package Type	Description	Quantity
SOT23-6	Tape and Reel	3000

Part Numbering



Part Marking



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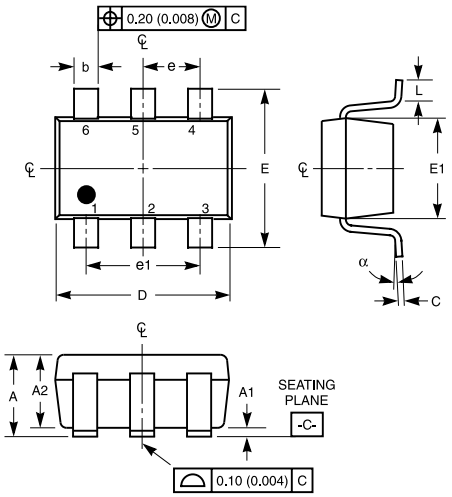
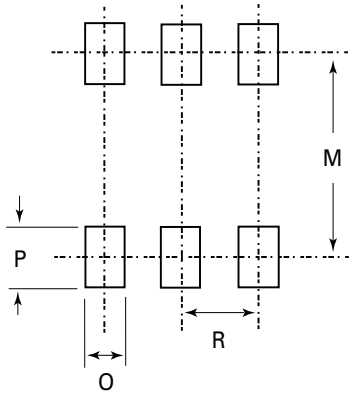
Dimensions - SOT23-6



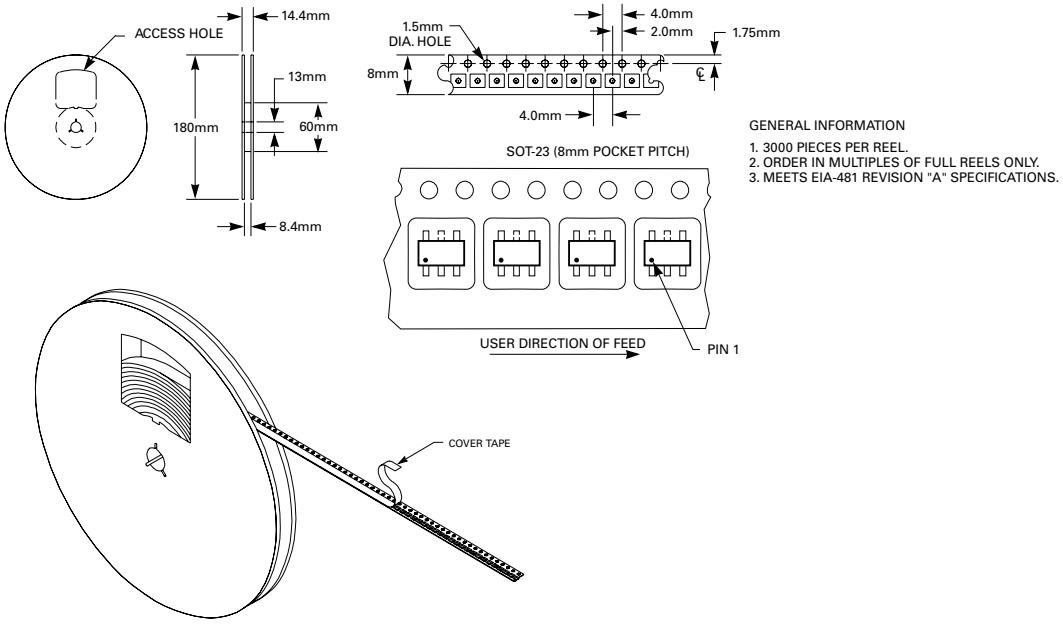
Recommended Solder Pad Layout



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	-	0.057	-	1.450
A1	-	0.006	-	0.150
A2	-	0.051	-	1.300
b	0.014	0.020	0.350	0.508
C	0.004	0.008	0.090	0.200
D	0.110	0.118	2.800	3.000
E	0.102	0.118	2.600	3.000
E1	0.057	0.069	1.450	1.750
e	-	0.037	-	0.950
e1	-	0.075	-	1.900
L (note 4.5)	0.004	0.023	0.100	0.600
N (note 6)	6		6	
α	0°C	10°C	0°C	10°C
M	-	0.102	-	2.590
O	-	0.027	-	0.690
P	-	0.039	-	0.990
R	-	0.038	-	0.950

Notes:
1. Dimensioning and tolearances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992)
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Foot lenth L measured at reference to seatng plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Embossed Carrier Tape & Reel Specification - SOT23-6



GENERAL INFORMATION
1. 3000 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revised: 09/12/16